ERRATA – ALL CHAPTERS

LOGIC AND COMPUTER DESIGN FUNDAMENTALS – 2nd Edition

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Introduction

The errata are given with reference to the printings of the book. The printing of your book is the last number in the string of numbers below "Printed in ..." on the page following the title page. For example: 10 9 8 7 6 5 4 3 2 is printing 2. Only those errors believed to affect technical correctness or understanding are listed.

Chapter 1: Printing 1

Page 24. **Problem 1-10.** Equation should be:

$$(N)_{10} = ((\ldots((A_{n-1}r + A_{n-2})r + A_{n-3})\ldots + A_2)r + A_1)r + A_0$$

Chapter 1: Printing 2

Page 24. **Problem 1-10.** Equation should be:

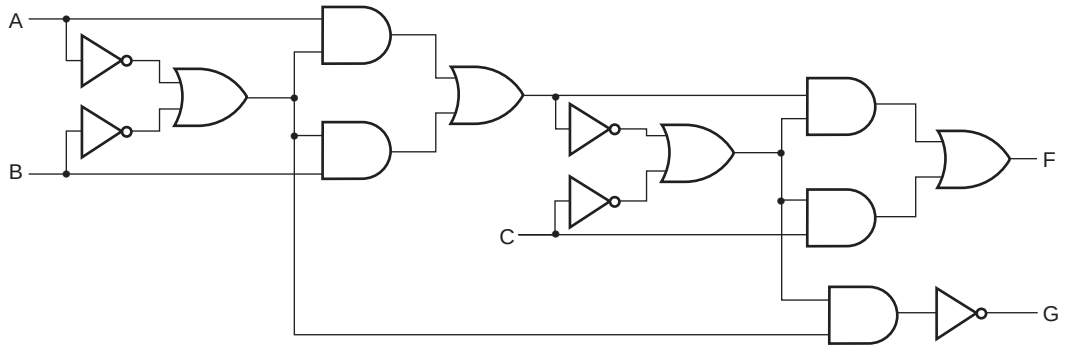
$$(N)_{10} = ((\ldots((A_{n-1}r + A_{n-2})r + A_{n-3})\ldots + A_2)r + A_1)r + A_0$$

Chapter 2: Printing 1

Page 84. **Problem 2-4.** $A \cdot B = 0$ and $A + B = 1$ should be $A \cdot B = 0$ and $A + B = 1$.

Page 87. **Problem 2-31.** "2-25" should be "2-27" and "2-27" should be "2-29."

Page 88. **Figure 2-46.** Variables on right and left missing. Should be:



Page 89. **Problem 2-41.** "delay to find t_{PHL}." should be "delay to find t_{pd}."

Chapter 3: Printing 1

Page 159 (Added 11/28/99). **Figure 3-44, Lines 14 through 17**. Replace `E_n` with `E`.

Page 162. **Figure 3-46.** The "comment" designation for the line numbers on the right should be `//` instead of `--`.

Page 176. **Problem 3-47.** "whether they are equal." should be "whether B is greater than A."

Page 177. **In paragraph marked with**  . "kime" should be "mano."

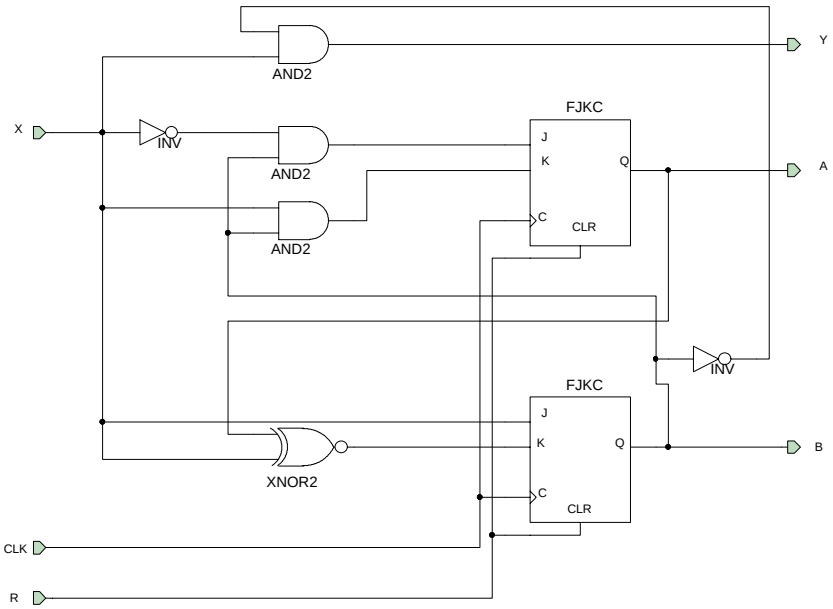
Page 177. **Problem 3-56.** "given in Appendix A." should be "given in the Companion Website Gallery."

Chapter 3: Printing 2

Page 159 (Added 11/28/99). **Figure 3-44, Lines 14 through 17**. Replace `E_n` with `E`.

Chapter 4: Printing 1

Page 222. **Figure 4-28.** Labels on flip-flops missing. Should be:



Page 235. **Line 4 from bottom.** "`end case;`" should be "`endcase`"

Page 245. **Problem 4-31.** "Table 4-6." should be "Table 4-7."

Page 246. **Problem 4-39.** Line 3 - "when D was" should be "when EN was" and Line 6 - "while EN = 1." should be "when EN becomes 1."

Page 247. **Optional Change: Problems 4-41, 4-42, and 4-43.** Delete the sentence "Use the D flip-flop ..." (This change appears in the 2nd and subsequent printings to improve the instructional value of these problems.)

Page 247. **Problem 4-46.** Line 3 - "when D was" should be "when EN was" and Line 6 - "while EN = 1." should be "when EN becomes 1."

Page 247. **Optional Change: Problems 4-48, 4-49, and 4-50.** Delete the sentence "Use the D flip-flop ..." (This change appears in the 2nd and subsequent printings to improve the instructional value of these problems.)

Chapter 5: Printing 1

Page 283. **Problem 5-29.** "*" added. (Solution will appear on the Web.)

Page 284. **Problem 5-31.** "problem 5-30" should be "problem 5-29."

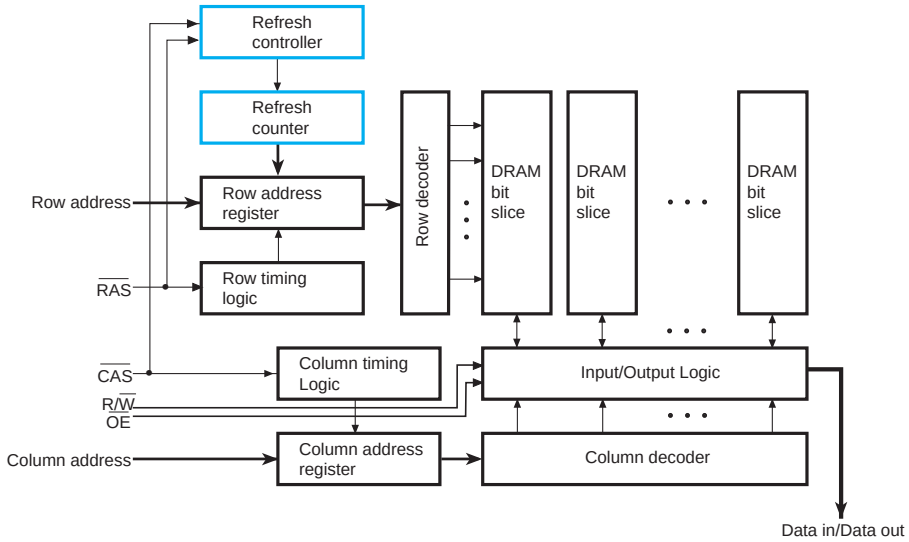
Page 284. **Problem 5-32.** "problem 5-31" should be "problem 5-30."

Page 284. **Problems 5-33, 5-35 and 5-39.** "*" added. (Solutions will appear on the Web.)

Page 284. **Problem 5-34 and Problem 5-40.** "D" should be "JK."

Chapter 6: Printing 1

Page 303. **Figure 6-13.** Outlines missing for Refresh Controller and Refresh Counter. Should be:



Page 336. **Problems 6-15.** "*" added. (Solutions will appear on the Web.)

Page 337. **Problems 6-18.** "*" added. (Solutions will appear on the Web.)

Chapter 7: Printing 1

Page 363 (Added 11/27/99). **Line 2.** "Whenever C_{in} is 1, $Y + B$ has 1 added." should be "Whenever C_{in} is 1, $A + Y$ has 1 added."

Page 375. **Figure 7-20.** Signal AA is 0 instead of 6 in clock cycle 2; signal BA is 6 instead of 0 in clock cycle 2. (BA remains 0 for clock cycles 3 and 4.)

Page 383 (Added 11/27/99). **Problem 7-3.** Interchange statements "Transfer R1 to R2" and "Clear R2 synchronously with the clock."

Page 386. **Problem 7-16.** "R9 <- R7" should be "R9 <- R1."

Chapter 7: Printing 2

Page 363 (Added 11/27/99). **Line 2.** "Whenever C_{in} is 1, $Y + B$ has 1 added." should be "Whenever C_{in} is 1, $A + Y$ has 1 added."

Page 383 (Added 11/27/99). **Problem 7-3.** Interchange statements "Transfer R1 to R2" and "Clear R2 synchronously with the clock."

Chapter 8: Printings 1 and 2.

Page 444 (Added 11/27/99). **Table 8-11.** Although the microprogram will function correctly as given, the entry EX0 in row IF and column NXT ADD is unnecessary, as is the corresponding entry 193 in **Table 8-12**.

Page 460 (Added 11/27/99). **Problem 8-11.** "Problem 8-6" should be "Problem 8-6(a)."

Page 461 (Added 11/27/99). **Problem 8-21.** "A", "B" and "C" should be "ST1", "ST2" and "ST3", respectively.

Chapter 9: Printing 1

Page 476. **Figure 9-2.** Box missing around "D."

Page 509. **Problem 9-28(a).** "2's complement" should be "signed 2's complement."

Chapter 10: Printings 1 and 2 (Added 11/28/99)

Page 520. **Line 6 from bottom.** "14-bit" should be "5-bit". This matches the width of the SB field used as the source of the constant. There is also a problem with conflicting use of the SB field. When it is used as a constant with the 1 in the most significant bit SB_4, the register address used for the destination can be affected. To avoid this problem, a 2-input AND can be added in Figure 10-4 between SB_4 and the S input to the 2-to-1 MUX. The other input to this AND is $\overline{MB(1)}$, forcing DSA_3 to control register address selection independently of SB_3 and SB_4 whenever SB is used for a constant.

Page 521 Added 12/7/99. **Figure 10-5.** On the S input, "3" should be "4."

Page 525. **Figure 10-8.** Field MS should be four bits, bits 26 through 23.

Page 527. **Bottom line.** Below, add the line:
"ANDing *RWE* with the signal otherwise driving *RW* on the register file, we cause"

Page 530. Added 12/7/99. **Figure 10-10(a).** "OPCODE[5:4]" should be "OPCODE[5:3]."

Page 530. Changed 12/7/99. **Figure 10-10(b).** "OPCODE[5:3] is correct. Below "OPCODE[5:3]" number of lines should be "3," not "2."

Page 531. **Top line.** Above, add the two lines:
"with the value stored in the *C* status bit and enables update of the *PSR*. The C_{in} replacement is needed for the ADDC and SUBB instructions. So that information"

Page 531. **Line 9.** "Section 8-9" should be "Section 8-11."

Page 539. Added 12/7/99. **Table 10-14.** Replace last six lines by:

Sym Add	Register Transfer Description	MC	MM /LS	MR /PS	DSA /MS	SB	MA	MB	MD	FS /NA	MO
SHR0	$R9 \leftarrow SD$	0	0	0	09	0D	0	0	0	10	0
SHR1	$R9 \leftarrow R9$ (Set MSTS)	0	0	0	09	0	0	0	0	00	F
SHR2	z:$CAR \leftarrow SHR6$	3	0	0	6	00	0	0	0	SHR6	0
SHR3	$DD \leftarrow 0 \parallel DD(15{:}1)$	0	0	0	0F	0F	0	0	0	11	0
SHR4	$R9 \leftarrow R9 - 1$	0	0	0	09	00	0	0	0	06	F
SHR5	$\bar{z}$: $CAR \leftarrow$ SHR3	3	0	1	6	00	0	0	0	SHR3	0
SHR6	$DD \leftarrow DD$, $CAR \leftarrow$ WB0(ROM)	2	1	4	0F	00	0	0	0	00	D

This shaded changes relate to the setting of MSTS and PSR. The added microinstruction SHR1 is necessary, since in SHR0, SD does not pass through the ALU, so cannot generate the necessary MSTS values. The change in SHR2 permits an exit from the routine while at the same time setting the PSR values for the shift operation.

Page 544. **Table 10-19.** For the last four instructions, "*PC* + se *IM*" should be "*PC* + 1 + se *IM*"

Page 546. **Line12.** "Section 8-9" should be "Section 8-11."

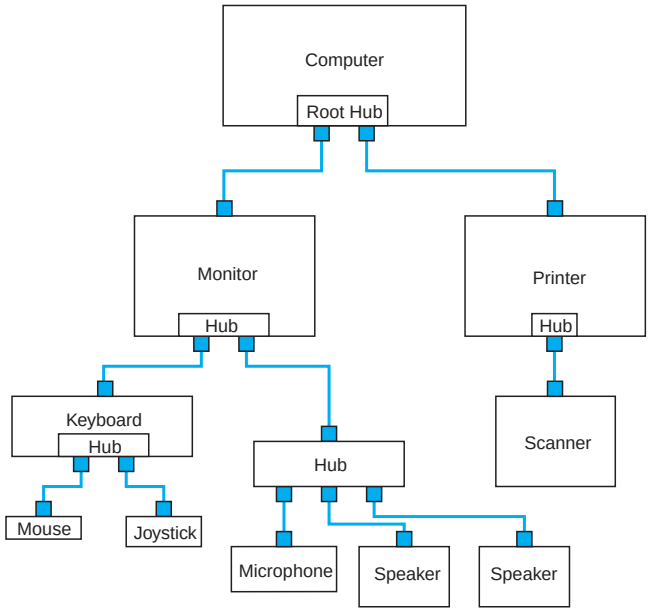
Page 546. **Lines 15 and 18. "**Figure 8-30" should be "Figure 8-34."

Page 550. **Line 5 from bottom. "**Figure 8-19" should be "Figure 8-23."

Page 557. **Figure 10-19.** The buses into 0 and 1 on MUX D' should to be interchanged. PC_{-1} into MUX A is not connected to Bus D'. The gap between Bus B and the right input to the Adder should be closed.

Chapter 11: Printing 1

Page 591. **Figure 11-10.** Connections missing between components. Should be:



Page 611. **Problem 11-8.** “c” and “d” should be “a” and “b” respectively.

Chapter 11: Printing 2

Page 611. **Problem 11-8.** “c” and “d” should be “a” and “b” respectively.

Chapter 12: Printing 1

None, so far.

If You Find Additional Errors

Please mail additional errors found or comments to:

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Thanks very much to the faculty and students sending in corrections to the first and second editions!

CRK